IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	: 10/005,483	Confirmation No.:	7202
Applicant	: James L. SNELL		
Filed	: 11/09/2001		
Title	: High Data Rate Spread Spectrum Transceiver And Associated Methods		
TC/Art Unit	: 2634		
Examiner:	: Ted Wang	Docket No.:	56162.000489
Customer No.	: **21967**		

PETITION UNDER 37 C.F.R. § 1.47(A)

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The above-identified reissue application has been accorded 37 C.F.R. § 1.47(a) status with respect to non-signing inventor James Snell. (see PTO Petition Grant attached as Exhibit 1). Due to recently discovered defects in the original reissue declaration and in view of the substantial amendments made to the newly added claims of the reissue application, the PTO is now requiring another original reissue declaration by inventors. However, after making a diligent attempt as described below, another of the named inventors, Victor Lucas, can not be reached and therefore is non-signing. The facts are as follows:

1. During multiple telephone conversations with Special Programs Examiner Krista Zele from the period of March 1, 2006 until April 12, 2006, it was determined that a new reissue declaration would be required. The May 5, 2006 Quayle Action reiterated this requirement.

2. Because § 1.47(a) status had already been granted with respect to inventor James Snell, it was only necessary to receive signatures from co-inventors Victor (Leonard) Lucas and Carl Andren.

3. On April 13, 2006 a letter was sent via Federal Express to Mr. Andren including the reissue declaration and the latest version of the claims as they were amended during prosecution of the reissue application. A copy of this letter and attachment is attached hereto as Exhibit 2. Our letter to Mr. Andren was received and returned to us in the prepaid Federal Express envelope provided. The original signed Reissue Declaration by Inventors signed by Inventor Carl Andren is enclosed as Exhibit 3.

4. On July 5, 2006 we also sent a letter to Victor Lucas via Federal Express including the reissue declaration and amended claims. Mr. Lucas' last known location is in Washington State. After obtaining a list of all the Victor L. and L. Victor Lucas' in Washington State, and calling those that had published numbers, we were unable to reach with Mr. Lucas. The telephone number at the last listed address is an unlisted number. Thus, we sent the letter without discussing the matter with Mr. Lucas by telephone to the following address:

Victor L. Lucas
7106 SE Sedgwick
Port Orchard, WA 98366

The letter to Mr. Lucas along with a copy of the Federal Express receipt is attached as Exhibit 4. We confirmed with the Kitsap County, Washington land records department that Mr. Lucas is registered at above address. A copy of the tax record for the above address is attached as Exhibit 5.

5. We therefore respectfully request that § 1.47(a) status also be granted with respect to inventor Victor Lucas and that application be allowed to be made by inventor Carl Andren on behalf of himself and the other inventors.

6. I, Phillip D. Mancini, Applicants representative, hereby submit that the above record is a true and accurate statement of the facts regarding our attempt to obtain the signature of co-inventor Victor Lucas. Prompt grant of the petition and issuance are respectfully requested.

Applicants believe that no additional charges beyond those paid by check are due in connection with this amendment. However, in the event Patent Office charges are due, please charge the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,

HUNTON & WILLIAMS

Date: Monday, August 7, 2006 By: _____

Phillip D. Mancini
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UNITED STATES PATENT AND TRADEMARK OFFICE

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Paper No. 9

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FEB 2 8 2003

OFFICE OF PETITIONS

In re
James L. Snell, Carl F. Andren and
Leonard Victor Lucas
Reissue Application No. 10/005,483
Filing Date: November 9, 2001
Reissue of Patent No. 5,982,807
Original Issue Date: November 9, 1999
Attorney Docket No. 125.003USR1

DECISION ACCORDING STATUS
UNDER § 1.47(a)

This is a decision on the "Renewed Petition under 37 CFR 1.47(b)" resubmitted by facsimile transmission on February 10, 2003. Petitioner has submitted *prima facie* evidence in the form of a stamped return postcard receipt that this renewed petition, though not of record in the application, was timely filed on December 2, 2002[1].

The petition is GRANTED.

The above-identified reissue application of patent No. 5,982,807 (Issued November 9, 1999) was filed on November 9, 2001, with an unexecuted reissue declaration; missing both the written consent of assignee with statement under 37 CFR 3.73(b),and the statutory basic filing fee; and with additional claim fees due. In response to a "Notice to File Missing Parts of Reissue Application" mailed February 8, 2002, petitioner timely filed the initial petition under § 1.47(b), asserting that status under § 1.47 is proper because sole inventor Snell refuses to join in the application. The petition was dismissed for failure to submit an acceptable declaration in compliance with § 1.175; and consequently, failure to show that inventor Snell refused to join in the application after having been presented with a proper reissue declaration for signature[2].

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[1] A postcard receipt which itemizes and properly identifies the items which are being filed serves as prima facie evidence of receipt in the USPTO of all the items listed thereon on the date stamped thereon by the USPTO. See MPEP 503. Petitioner's postcard is date-stamped December 2, 2002 by the USPTO, and specifically itemizes as being filed a renewed petition under § 1.47 (and supporting documentation) and a one-month extension of time. (Finance records show payment of the extension of time fee in December of 2002).

[2] A grantable petition under 37 CFR §1.47(b) requires: (1) an acceptable oath or declaration in compliance with 37 C.F.R. § 1.63 and 1.64 or 1.175; (2) the rule 47 applicant must state his or her relationship to the inventor as required by 37 C.F.R. § 1.64; (3) proof that the non-signing inventor cannot be found or reached after diligent effort, or refuses to sign the oath or declaration after having been presented with the application papers (specification, claims and drawings); (4) the petition fee; (5) a statement of the last known address of the non-signing inventor; (6) that rule 47 applicant make out a *prima facie* case (i) that the invention has been assigned to him or her or (ii) that the inventor has agreed in writing to assign the invention to him or her or (iii) otherwise demonstrate a proprietary interest in the subject matter of the invention; and (7) rule 47 applicant must prove that the filing of the application is necessary (i) to preserve the rights of the parties or (ii) to prevent irreparable damage.

On instant renewed petition, petitioner submitted a reissue declaration executed by joint inventors Carl Andren and Leonard Lucas. It is preliminarily noted that this petition is now considered under 37 CFR 1.47(a). Filing under 37 CFR 1.47(b) and 35 U.S.C. 118 is permitted only when no inventor is available to make application. In this instance, inventors Andren and Lucas are available.

A grantable petition under § 1.47(a) requires: (1) an acceptable oath or declaration in compliance with 37 C.F.R. § 1.63 and 1.64 or 1.175; (2) proof that the non-signing inventor cannot be found or reached after diligent effort, or refuses to sign the oath or declaration after having been presented with the application papers (specification, claims and drawings); (3) a statement of the last known address of the non-signing inventor, and (4) the petition fee. On initial petition, petitioner satisfied requirements (3) and (4).

On instant renewed petition, petitioner satisfied requirements (1) and (2). The declaration submitted on instant renewed petition has been reviewed and found in compliance with §§ 1.175 and 1.47(a). An oath or declaration signed by all the available joint inventors with the signature block of the non-signing inventor(s) left blank may be treated as having been signed by all the available joint inventors on behalf of the non-signing inventor(s), unless otherwise indicated. Accordingly, the instant declaration is accepted as being executed by available joint inventors Andren and Lucas on behalf of themselves and on behalf of non-signing inventor Snell.

Furthermore, with the instant renewed petition, petitioner submitted proof that non-signing inventor Snell has refused to join in this reissue application after having been presented with the application papers (including the proper reissue declaration). This evidence includes the first hand declarations of Elizabeth Bauer, detailing the presentation of the reissue declaration and application papers to non-signing inventor Snell; and of David Fogg, detailing inventor Snell's subsequent refusal to sign the reissue declaration. Copies of the letters (and mailing labels) transmitting by Federal Express and requesting presentation by hand-delivery (process server) of the application papers to non-signing inventor Snell; and a declaration of the process server, attesting to having served inventor Snell with the papers were made a part of the statements.

In view thereof, this application is hereby accorded Rule 1.47(a) status.

As provided in new Rule 1.47(c), this Office will forward notice of this application's filing to the non-signing inventor at the address given in the petition. Notice of the filing of this application will also be published in the Official Gazette.

The application file is being forwarded to Technology Center 2631 for examination in due course.

Telephone inquiries regarding this decision should be directed to the undersigned at (703) 305-0309.

Nancy Johnson

Nancy Johnson
Petitions Attorney
Office of Petitions

UNITED STATES PATENT AND TRADEMARK OFFICE
SPECIAL PROGRAM LAW OFFICE/OFFICE OF PETITIONS

FACSIMILE TRANSMISSION

DATE: Feb 28, 2003

125.0034SR1

TO: David Foss
(NAME)

612-677-3553
(FACSIMILE NUMBER)

PTO
(ORGANIZATION)

612 332-4720
(TELEPHONE NUMBER)

SENDER: [signature]
(NAME)

TOTAL NUMBER OF PAGES _____ (INCLUDING THIS COVER PAGE)

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DIRECT TELEPHONE NO.: 703-305-9282 FACSIMILE NO.: 703-308-6916

Brief Message:

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HUNTON & WILLIAMS LLP
1751 PINNACLE DRIVE
SUITE 1700
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PHILLIP MANCINI
DIRECT DIAL: 703-714-7554
EMAIL: pmancini@hunton.com

FILE NO: 56162.000489

April 13, 2006

Via Overnight Delivery

Carl F. Andren
906 S. Ramona Avenue
Indialantic, Florida 32903

Re: U.S. Reissue Patent Application No. 10/005,483
Title: "High Data Rate Spread Spectrum Transceiver and Associated Methods"
Inventors: James Leroy Snell et al.
Your Reference: GV 289 (W)
Our Reference: 56162.000489

Dear Carl:

Enclosed please find a Declaration and current set of claims for the above-identified reissue application. In order to get this application to issue as a patent we need to submit an additional declaration including the signatures of Carl Andren and Victor Lucas. Therefore, please execute the enclosed declaration by signing and dating at the specified location and return it to us in the enclosed pre-paid Fedex return envelope.

It is imperative that we get this declaration filed in the Patent Office within the next week. Thank you for your cooperation in this matter. Please feel free to call me with any questions or concerns.

Sincerely,

Phillip Mancini
Sent on behalf of Kevin T. Duncan

KTD/PDM:gjc
Enclosures

PTO/SB/51 (04-05)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) 56162.000489

I hereby declare that:
Each inventor's residence, mailing address and citizenship are stated below next to their name.
I believe the inventors named below to be the original and first inventor(s) of the subject matter which is described and claimed in patent number 5,982,807, granted November 9, 1999 and for which a reissue patent is sought on the invention entitled High Data Rate Spread Spectrum Transceiver and Associated Methods,

the specification of which

☐ is attached hereto.

☒ was filed on 11/09/2001 as reissue application number 10/005,483

and was amended on 11/09/01; 08/28/02; 10/23/02; 12/02/02; 06/19/03; 03/05/04; 11/09/04; and 09/29/05.
(If applicable)

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

☐ I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b). Attached is form PTO/SB/02B (or equivalent) listing the foreign applications.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, such must be stated with an explanation as to the nature of the broadening:

This reissue application is based on an error in that the applicant and applicant's attorney failed to appreciate the full scope of the invention and thus claimed less subject matter than could have been claimed. The issued claims contain limitations that are not essential for practicing the broad teachings of the invention disclosed in the application. Thus, this reissue application is intended as a broadening reissue.

In one example of this error, in issued patent claim 2, Applicant employed means plus function language. The new claims presented in this reissue application avoid the use of means plus function language and thus broaden the scope of the invention.

PTO/SB/51 (04-05)
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(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional): 56162.000489

All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant.

Note: To appoint a power of attorney, use form PTO/SB/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 21967

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

Full name of sole or first inventor (given name, family name)
James Leroy Snell

Inventor's signature	Date
Residence 2695 Lemon Street, NE, Palm Bay, Florida 32905	Citizenship U.S.
Mailing Address Same as above	

Full name of second joint inventor (given name, family name)
Carl F. Andren

Inventor's signature	Date
Residence 906 S. Ramona Avenue, Indialantic, Florida 32903	Citizenship U.S.
Mailing Address Same as above	

Full name of third joint inventor (given name, family name)
Leonard Victor Lucas

Inventor's signature	Date
Residence 11529 Greenwood Ave., N, Apt. 6, Seattle, WA 98133	Citizenship U.S.
Mailing Address Same as above	

☐ Additional joint inventors or legal representative(s) are named on separately numbered sheets forms PTO/SB/02A or 02LR attached hereto

PATENT
56162.000489

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	: 10/005,483	Confirmation No.:	7202
Applicant	: James L. SNELL		
Filed	: 11/09/2001		
Title	: High Data Rate Spread Spectrum Transceiver And Associated Methods		
TC/Art Unit	: 2634		
Examiner:	: Ted Wang	Docket No.:	56162.000489
Customer No.	: **21967**		

SUPPLEMENTAL AMENDMENT

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to the Notice of Appeal filed on September 29, 2005, and in response to the March 1 and March 31 telephone conferences with Special Programs Examiner Krista Zele, Applicant hereby submits a Supplemental Amendment in accordance with the formal requirements of 37 C.F.R. § 1.121. This Amendment does not make any substantive changes to the claims but rather only updates the claim listing so that claim amendments already of record are shown with respect to the issued claims rather than with respect to previous amendments made during prosecution of this reissue application. Entry of the Amendment is therefore respectfully requested

Please consider the following:

Amendments to the Claims, as shown in the following Listing of Claims; and

Remarks.

Listing of the Claims

1. (Twice Amended) A spread spectrum radio transceiver comprising:

a baseband processor and a radio circuit connected thereto, said baseband processor comprising

a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit,

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to said radio circuit,

said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code having a reduced DC component for reducing an average DC signal component [which]of the information decoded by the modified Walsh code relative to that information being decoded by an unmodified Walsh code which, in combination with the AC-coupling to said at least one A/D converter enhances overall performance, and

a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

2. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

3. (Original) A spread spectrum radio transceiver according to claim 2 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

4. (Original) A spread spectrum radio transceiver according to claim 3 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

5. (Original) A spread spectrum radio transceiver according to claim 3 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

6. (Original) A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

7. (Original) A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

8. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.

9. (Original) A spread spectrum radio transceiver according to claim 1 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

10. (Original) A spread spectrum radio transceiver according to claim 1 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel connected correlators connected to said modified Walsh function generator.

11. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

12. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

13. (Original) A spread spectrum radio transceiver according to claim 1 wherein said demodulator comprises clear channel assessing means for generating a clear channel assessment signal.

14. (Original) A spread spectrum radio transceiver according to claim 1 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator connected to said baseband processor; and

an up/down frequency converter connected to said quadrature intermediate frequency modulator/demodulator.

15. (Original) A spread spectrum radio transceiver according to claim 14 wherein said radio circuit further comprises:

a low noise amplifier having an output connected to an input of said up/down converter; and

a radio frequency power amplifier having an input connected to an output of said up/down converter.

16. (Original) A spread spectrum radio transceiver according to claim 15 further comprising:

an antenna; and

an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

17. (Three Times Amended) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to receive information;

said demodulator comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component [to thereby increase]of the information decoded by the predetermined orthogonal code relative to that information being decoded by the predetermined

orthogonal code in its unmodified state to thereby promote AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one predetermined orthogonal code function encoder for encoding information according to the predetermined orthogonal code.

18. (Original) A baseband processor according to claim 17 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

19. (Original) A baseband processor according to claim 18 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

20. (Original) A baseband processor according to claim 19 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

21. (Original) A baseband processor according to claim 19 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

22. (Original) A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

23. (Original) A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

24. (Original) A baseband processor according to claim 17 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder.

25. (Original) A baseband processor according to claim 17 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

26. (Original) A baseband processor according to claim 17 wherein the predetermined orthogonal code is a bi-orthogonal code.

27. (Original) A baseband processor according to claim 17 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

28. (Original) A baseband processor according to claim 17 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

29. (Original) A baseband processor according to claim 17 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

30. (Original) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

means for operating in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate,

header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising

at least one correlator for decoding received information,

means for operating in one of the first and second formats,

header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header,

a first carrier tracking loop for the third format, and

a second carrier tracking loop for the first and second formats.

31. (Original) A baseband processor according to claim 30 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

32. (Original) A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

33. (Original) A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

34. (Original) A baseband processor according to claim 30 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

35. (Original) A baseband processor according to claim 30 wherein said modulator comprises a scrambler; and

wherein said demodulator comprises a descrambler.

36. (Twice Amended) A modulator for a spread spectrum radio transceiver, said modulator comprising:

modulator means for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator means comprising at least one predetermined orthogonal code function encoder for encoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the predetermined orthogonal code relative to that information being encoded by the predetermined orthogonal code in its unmodified state.

37. (Original) A modulator according to claim 36 wherein said modulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

38. (Original) A modulator according to claim 37 wherein said modulator means comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats.

39. (Original) A modulator according to claim 38 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

40. (Original) A modulator according to claim 36 wherein said modulator means further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder, and wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

41. (Original) A modulator according to claim 36 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

42. (Original) A modulator according to claim 36 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

43. (Original) A modulator according to claim 36 wherein the predetermined orthogonal code is a bi-orthogonal code.

44. (Three Times Amended) A demodulator for a spread spectrum radio transceiver, said demodulator comprising:

demodulator means for spread spectrum phase shift keying (PSK) demodulating information received from [said]a radio circuit, said demodulator means comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC signal component for reducing an average DC signal component of the information decoded by the predetermined orthogonal code relative to that information being decoded by the predetermined orthogonal code in its unmodified state.

45. (Original) A demodulator according to claim 44 wherein said demodulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

46. (Original) A demodulator according to claim 45 wherein said demodulator means comprises header demodulator means for demodulating data packets including a header in a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

47. (Original) A demodulator according to claim 46 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

48. (Original) A demodulator according to claim 46 wherein said demodulator means further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

49. (Original) A demodulator according to claim 48 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

50. (Original) A demodulator according to claim 48 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

51. (Original) A demodulator according to claim 44 further comprising means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits).

52. (Original) A demodulator according to claim 44 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

53. (Original) A demodulator according to claim 44 wherein the predetermined orthogonal code is a bi-orthogonal code.

54. (Original) A demodulator according to claim 44 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

55. (Twice Amended) A method for baseband processor for spread spectrum radio communication, the method comprising the steps of:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the predetermined orthogonal code relative to that information being encoded by the predetermined orthogonal code in its unmodified state ; and

spread spectrum PSK demodulating received information by decoding the received information according to the predetermined orthogonal code.

56. (Original) A method according to claim 55 further comprising the step of AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

57. (Original) A method according to claim 55 further comprising the steps of modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

58. (Original) A method according to claim 57 further comprising the steps of:

modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

59. (Original) A method according to claim 58 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

60. (Original) A method according to claim 55 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

61. (Original) A method according to claim 55 wherein the predetermined orthogonal code is a bi-orthogonal code.

62. (New) A spread spectrum radio transceiver comprising:

a baseband processor and a radio circuit coupled thereto, said baseband processor comprising a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit, at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to said radio circuit, said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code having a reduced DC component relative to an unmodified Walsh code for reducing an average DC signal component of the information decoded by the modified Walsh code relative to that information being decoded by the Walsh code in its unmodified state, and a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

63. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data

rate; and wherein said demodulator is configured to operate in one of the first and second formats.

64. (New) A spread spectrum radio transceiver according to claim 63 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

65. (New) A spread spectrum radio transceiver according to claim 64 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

66. (New) A spread spectrum radio transceiver according to claim 64 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

67. (New) A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of

said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

68. (New) A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

69. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.

70. (New) A spread spectrum radio transceiver according to claim 62 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

71. (New) A spread spectrum radio transceiver according to claim 62 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel coupled correlators coupled to said modified Walsh function generator.

72. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is

configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

73. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

74. (New) A spread spectrum radio transceiver according to claim 62 wherein said demodulator is configured to generate a clear channel assessment signal.

75. (New) A spread spectrum radio transceiver according to claim 62 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator coupled to said baseband processor; and

an up/down frequency converter coupled to said quadrature intermediate frequency modulator/demodulator.

76. (New) A spread spectrum radio transceiver according to claim 75 wherein said radio circuit further comprises:

a low noise amplifier having an output coupled to an input of said up/down converter; and

a radio frequency power amplifier having an input coupled to an output of said up/down converter.

77. (New) A spread spectrum radio transceiver according to claim 76 further comprising:

an antenna; and

an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

78. (New) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;

at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to receive information;

said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information decoded by the orthogonal code relative to that information being decoded by the orthogonal code in its unmodified state to thereby promote AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one orthogonal code function encoder for encoding information according to the orthogonal code.

79. (New) A baseband processor according to claim 78 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein

said demodulator is configured to operate in one of the first and second formats.

80. (New) A baseband processor according to claim 79 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

81. (New) A baseband processor according to claim 80 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

82. (New) A baseband processor according to claim 80 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

83. (New) A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

84. (New) A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

85. (New) A baseband processor according to claim 78 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder.

86. (New) A baseband processor according to claim 78 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

87. (New) A baseband processor according to claim 78 wherein the orthogonal code is a bi-orthogonal code.

88. (New) A baseband processor according to claim 78 wherein said at least one orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

89. (New) A baseband processor according to claim 78 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to

generate a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

90. (New) A baseband processor according to claim 78 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

91. (New) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

wherein said modulator is configured to operate in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate, and

wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising at least one correlator for decoding received information, wherein said demodulator is configured to operate in one of the first and second formats, wherein said demodulator is configured to demodulate data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data

after the header, a first carrier tracking loop for the third format, and a second carrier tracking loop for the first and second formats.

92. (New) A baseband processor according to claim 91 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

93. (New) A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

94. (New) A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

95. (New) A baseband processor according to claim 91 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is further configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

96. (New) A baseband processor according to claim 91 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

97. (New) A modulator for a spread spectrum radio transceiver, said modulator configured to modulate information for transmission by spread spectrum phase shift keying (PSK), said modulator comprising at least one orthogonal code function encoder for encoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the orthogonal code relative to that information being encoded by the orthogonal code in its unmodified state.

98. (New) A modulator according to claim 97 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

99. (New) A modulator according to claim 98 wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats.

100. (New) A modulator according to claim 99 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

101. (New) A modulator according to claim 97 wherein said modulator is configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder, and wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

102. (New) A modulator according to claim 97 wherein said at least one orthogonal code function correlator comprises:

an orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

103. (New) A modulator according to claim 97 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

104. (New) A modulator according to claim 97 wherein the orthogonal code is a bi-orthogonal code.

105. (New) A demodulator for a spread spectrum radio transceiver, said demodulator configured to demodulate information by spread spectrum phase shift keying (PSK) demodulating information received from a radio circuit, said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the

information decoded by the orthogonal code relative to that information being decoded by the orthogonal code in its unmodified state.

106. (New) A demodulator according to claim 105 wherein said demodulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

107. (New) A demodulator according to claim 106 wherein said demodulator is configured to demodulate data packets including a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

108. (New) A demodulator according to claim 107 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

109. (New) A demodulator according to claim 107 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

110. (New) A demodulator according to claim 109 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

111. (New) A demodulator according to claim 109 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

112. (New) A demodulator according to claim 105 further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits).

113. (New) A demodulator according to claim 105 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

114. (New) A demodulator according to claim 105 wherein the orthogonal code is a bi-orthogonal code.

115. (New) A demodulator according to claim 105 wherein said at least one orthogonal code function correlator comprises:

an orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

116. (New) A method for spread spectrum radio communication, the method comprising:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the orthogonal code relative to that information being encoded by the orthogonal code in its unmodified state; and

spread spectrum PSK demodulating received information by decoding the received information according to the orthogonal code.

117. (New) A method according to claim 116 further comprising AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

118. (New) A method according to claim 116 further comprising modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

119. (New) A method according to claim 118 further comprising:

modulating data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and

demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

120. (New) A method according to claim 119 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

121. (New) A method according to claim 116 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

122. (New) A method according to claim 116 wherein the orthogonal code is a bi-orthogonal code.

123. (New) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence generated at a predetermined chip rate;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences generated at the same chip rate as said spreading sequence and chosen from a set that is substantially orthogonal with low DC components; and

applying the spread-spectrum encoded symbols of said header field and selected chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

124. (New) The method of claim 123 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit second data symbol and differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.

125. (New) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences chosen from a set that is substantially orthogonal with low DC components, each of said chip sequences being differentially phase encoded;

applying a reference phase based on encoding of the last of said first data symbols to the differential encoding of the first selected chip sequence; and

inputting said encoded symbols of said header field and said differentially encoded chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

126. (New) The method of claim 125 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit second data symbol and

differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.

127. (New) A method of generating an rf signal in a transmitter having a phase shift modulator with I and Q inputs comprising the steps of:

supplying a stream of binary information containing header data and payload data, said header data specifying at least a first payload data rate or a second payload data rate;

encoding said payload data when said header data specifies said first payload data rate by grouping said payload data into N-bit symbols, where N is greater than 1, and applying each N-bit symbol to select one of 2^N possible chip sequences and chosen from a set that is substantially orthogonal with low DC components;

encoding said payload data when said header data specifies said second payload data rate by grouping said payload data into 2N-bit symbols and applying each 2N-bit symbol to select one of 2^{2N} possible chip sequences; and

applying each selected chip sequence to the I and Q inputs of said phase shift modulator.

128. (New) The method of claim 127 wherein the chip sequences selectable by said 2N-bit symbols include the chip sequences selectable by said N-bit symbols plus 2^{2N}-2^N additional chip sequences.

129. (New) The method of claim 127 wherein the chip sequences selected by said N-bit symbols and said 2N-bit symbols are generated by selecting an initial chip sequence in accordance with a

first data segment of an N-bit or 2N-bit symbol and differentially phase encoding the selected initial chip sequence in accordance with a second data segment of the same N-bit or 2N-bit symbol.

130. (New) The method of claim 127 wherein each of the 2^{2N} chip sequences selectable by said 2N-bit symbols comprises an I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively.

131. (New) The method of claim 129 wherein N=4 and wherein each chip sequence selected by a 2N-bit symbol comprises an initial I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively, said initial I/Q chip sequence being selected by 6 bits of a 2N-bit symbol and being differentially phase encoded in accordance with the other 2 bits of the same 2N-bit symbol.

132. (New) A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:

grouping said binary data into N-bit symbols;

applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences, wherein each chip sequence is M chips in length and is a composite of an M-bit basic sequence and an M-bit modification sequence and chosen from a set that is substantially orthogonal with low DC components;

rotating the phase of the selected chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said chip sequence; and

transmitting each phase-rotated, selected chip sequence at said predetermined chip rate.

133. (New) A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:

grouping said binary data into N-bit symbols;

applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences chosen from a set that is substantially orthogonal with low DC components, wherein each chip sequence is M chips in length;

combining the selected basic chip sequence with a fixed, M-chip modification sequence to produce a selected M-chip composite chip sequence;

rotating the phase of the selected M-chip composite chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said basic chip sequence; and

transmitting each phase rotated, selected composite chip sequence at said predetermined chip rate.

Remarks

Claims 1-133 remain pending in this application and have been indicated as allowable. As noted above, this Supplemental Amendment does not make any changes to the claims but rather updates them to show amendments already made to the claims with respect to the issued patent claims as required of a reissue application under 37 C.F.R. § 1.121. Because the Amendment does not raise any new issues, entry is respectfully requested.

Applicant appreciates the Patent Office's indication that all pending claims 1-133 are allowable. However, in recognition of the minor formalities brought to Applicant's attention by Special Programs Examiner Zele, Applicant has amended the claims and respectfully submits that all formal matters have thereby been satisfied.

Should the Patent Office determine that anything further would be desirable in order to place this application in even better condition for allowance, the Office Personnel are invited to contact Applicant's undersigned representative at the telephone number listed below.

Applicants believe that no charges are due in connection with this amendment. However, in the event Patent Office charges are due, please charge the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,

Dated: March 31, 2006

By:_____
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FILE NO: 56162.000489

July 5, 2006

Via Overnight Delivery

Victor L. Lucas
7106 SE Sedgwick
Port Orchard, WA 98366

Re: U.S. Reissue Patent Application No. 10/005,483
Title: "High Data Rate Spread Spectrum Transceiver and Associated Methods"
Inventors: James Leroy Snell et al.
Your Reference: GV 289 (W)
Our Reference: 56162.000489

Dear Victor:

Enclosed please find a Declaration and current set of claims for the above-identified reissue application. In order to get this application to issue as a patent we need to submit an additional declaration including the signatures of Carl Andren and Victor Lucas. Therefore, please execute the enclosed declaration by signing and dating at the specified location and return it to us in the enclosed pre-paid Fedex return envelope.

It is imperative that we get this declaration filed in the Patent Office within the next month. Thank you for your cooperation in this matter. Please feel free to call me with any questions or concerns.

Sincerely,

Phillip Mancini
Sent on behalf of Kevin T. Duncan

KTD/PDM:gjc
Enclosures

PTO/SB/51 (04-05)
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REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) 56162.000489

I hereby declare that:
Each inventor's residence, mailing address and citizenship are stated below next to their name.
I believe the inventors named below to be the original and first inventor(s) of the subject matter which is described and claimed in patent number 5,982,807, granted November 9, 1999 and for which a reissue patent is sought on the invention entitled High Data Rate Spread Spectrum Transceiver and Associated Methods,

the specification of which

☐ is attached hereto.

☒ was filed on 11/09/2001 as reissue application number 10/005,483

and was amended on 11/09/01; 08/28/02; 10/23/02; 12/02/02; 06/19/03; 03/05/04; 11/09/04; and 09/29/05.
(If applicable)

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

☐ I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b). Attached is form PTO/SB/02B (or equivalent) listing the foreign applications.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, such must be stated with an explanation as to the nature of the broadening:

This reissue application is based on an error in that the applicant and applicant's attorney failed to appreciate the full scope of the invention and thus claimed less subject matter than could have been claimed. The issued claims contain limitations that are not essential for practicing the broad teachings of the invention disclosed in the application. Thus, this reissue application is intended as a broadening reissue.

In one example of this error, in issued patent claim 2, Applicant employed means plus function language. The new claims presented in this reissue application avoid the use of means plus function language and thus broaden the scope of the invention.

PTO/SB/51 (04-05)
Approved for use through 04/30/2007, OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

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All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant.

Note: To appoint a power of attorney, use form PTO/SB/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 21967

OR

☐ Firm or Individual Name					
Address					
City		State	Florida	Zip	32905
Country					
Telephone		Email			

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

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Inventor's signature	Date
Residence	Citizenship

Mailing Address

☐ Additional joint inventors or legal representative(s) are named on separately numbered sheets forms PTO/SB/02A or 02LR attached hereto.

PATENT
56162.000489

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	: 10/005,483	Confirmation No.:	7202
Applicant	: James L. SNELL		
Filed	: 11/09/2001		
Title	: High Data Rate Spread Spectrum Transceiver And Associated Methods		
TC/Art Unit	: 2634		
Examiner:	: Ted Wang	Docket No.:	56162.000489
Customer No.	: **21967**		

SUPPLEMENTAL AMENDMENT

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Further to the Notice of Appeal filed on September 29, 2005, and in response to the March 1 and March 31 telephone conferences with Special Programs Examiner Krista Zele, Applicant hereby submits a Supplemental Amendment in accordance with the formal requirements of 37 C.F.R. § 1.121. This Amendment does not make any substantive changes to the claims but rather only updates the claim listing so that claim amendments already of record are shown with respect to the issued claims rather than with respect to previous amendments made during prosecution of this reissue application. Entry of the Amendment is therefore respectfully requested

Please consider the following:

Amendments to the Claims, as shown in the following Listing of Claims; and

Remarks.

Listing of the Claims

1. (Twice Amended) A spread spectrum radio transceiver comprising:

a baseband processor and a radio circuit connected thereto, said baseband processor comprising

a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit,

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to said radio circuit,

said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code having a reduced DC component for reducing an average DC signal component [which]of the information decoded by the modified Walsh code relative to that information being decoded by an unmodified Walsh code which, in combination with the AC-coupling to said at least one A/D converter enhances overall performance, and

a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

2. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

3. (Original) A spread spectrum radio transceiver according to claim 2 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

4. (Original) A spread spectrum radio transceiver according to claim 3 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

5. (Original) A spread spectrum radio transceiver according to claim 3 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

6. (Original) A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

7. (Original) A spread spectrum radio transceiver according to claim 5 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

8. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.

9. (Original) A spread spectrum radio transceiver according to claim 1 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

10. (Original) A spread spectrum radio transceiver according to claim 1 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel connected correlators connected to said modified Walsh function generator.

11. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

12. (Original) A spread spectrum radio transceiver according to claim 1 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

13. (Original) A spread spectrum radio transceiver according to claim 1 wherein said demodulator comprises clear channel assessing means for generating a clear channel assessment signal.

14. (Original) A spread spectrum radio transceiver according to claim 1 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator connected to said baseband processor; and

an up/down frequency converter connected to said quadrature intermediate frequency modulator/demodulator.

15. (Original) A spread spectrum radio transceiver according to claim 14 wherein said radio circuit further comprises:

a low noise amplifier having an output connected to an input of said up/down converter; and

a radio frequency power amplifier having an input connected to an output of said up/down converter.

16. (Original) A spread spectrum radio transceiver according to claim 15 further comprising:

an antenna; and

an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

17. (Three Times Amended) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;

at least one analog-to-digital (A/D) converter having an output connected to said demodulator and an input AC-coupled to receive information;

said demodulator comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component [to thereby increase]of the information decoded by the predetermined orthogonal code relative to that information being decoded by the predetermined

orthogonal code in its unmodified state to thereby promote AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one predetermined orthogonal code function encoder for encoding information according to the predetermined orthogonal code.

18. (Original) A baseband processor according to claim 17 wherein said modulator comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein said demodulator comprises means for operating in one of the first and second formats.

19. (Original) A baseband processor according to claim 18 wherein said modulator comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

20. (Original) A baseband processor according to claim 19 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

21. (Original) A baseband processor according to claim 19 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

22. (Original) A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

23. (Original) A baseband processor according to claim 21 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

24. (Original) A baseband processor according to claim 17 wherein said modulator further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder.

25. (Original) A baseband processor according to claim 17 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

26. (Original) A baseband processor according to claim 17 wherein the predetermined orthogonal code is a bi-orthogonal code.

27. (Original) A baseband processor according to claim 17 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

28. (Original) A baseband processor according to claim 17 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

29. (Original) A baseband processor according to claim 17 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

30. (Original) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

means for operating in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate,

header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising

at least one correlator for decoding received information,

means for operating in one of the first and second formats,

header demodulator means for demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header,

a first carrier tracking loop for the third format, and

a second carrier tracking loop for the first and second formats.

31. (Original) A baseband processor according to claim 30 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

32. (Original) A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

33. (Original) A baseband processor according to claim 30 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

34. (Original) A baseband processor according to claim 30 wherein said modulator comprises spreading means for spreading each data bit using a pseudorandom (PN) sequence at a predetermined chip rate and preamble modulating means for generating a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

35. (Original) A baseband processor according to claim 30 wherein said modulator comprises a scrambler; and

wherein said demodulator comprises a descrambler.

36. (Twice Amended) A modulator for a spread spectrum radio transceiver, said modulator comprising:

modulator means for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator means comprising at least one predetermined orthogonal code function encoder for encoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the predetermined orthogonal code relative to that information being encoded by the predetermined orthogonal code in its unmodified state.

37. (Original) A modulator according to claim 36 wherein said modulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

38. (Original) A modulator according to claim 37 wherein said modulator means comprises header modulator means for modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats.

39. (Original) A modulator according to claim 38 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

40. (Original) A modulator according to claim 36 wherein said modulator means further comprises means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one predetermined orthogonal code function encoder, and wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

41. (Original) A modulator according to claim 36 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

42. (Original) A modulator according to claim 36 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

43. (Original) A modulator according to claim 36 wherein the predetermined orthogonal code is a bi-orthogonal code.

44. (Three Times Amended) A demodulator for a spread spectrum radio transceiver, said demodulator comprising:

demodulator means for spread spectrum phase shift keying (PSK) demodulating information received from [said]a radio circuit, said demodulator means comprising at least one predetermined orthogonal code function correlator for decoding information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC signal component for reducing an average DC signal component of the information decoded by the predetermined orthogonal code relative to that information being decoded by the predetermined orthogonal code in its unmodified state.

45. (Original) A demodulator according to claim 44 wherein said demodulator means comprises means for operating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

46. (Original) A demodulator according to claim 45 wherein said demodulator means comprises header demodulator means for demodulating data packets including a header in a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

47. (Original) A demodulator according to claim 46 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

48. (Original) A demodulator according to claim 46 wherein said demodulator means further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

49. (Original) A demodulator according to claim 48 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

carrier NCO control means for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

50. (Original) A demodulator according to claim 48 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

carrier loop filter control means for selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

51. (Original) A demodulator according to claim 44 further comprising means for partitioning data into four bit nibbles of sign (one bit) and magnitude (three bits).

52. (Original) A demodulator according to claim 44 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

53. (Original) A demodulator according to claim 44 wherein the predetermined orthogonal code is a bi-orthogonal code.

54. (Original) A demodulator according to claim 44 wherein said at least one predetermined orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel connected correlators connected to said predetermined orthogonal code function generator.

55. (Twice Amended) A method for baseband processor for spread spectrum radio communication, the method comprising the steps of:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to a predetermined orthogonal code, wherein the predetermined orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the predetermined orthogonal code relative to that information being encoded by the predetermined orthogonal code in its unmodified state ; and

spread spectrum PSK demodulating received information by decoding the received information according to the predetermined orthogonal code.

56. (Original) A method according to claim 55 further comprising the step of AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

57. (Original) A method according to claim 55 further comprising the steps of modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

58. (Original) A method according to claim 57 further comprising the steps of:

modulating data packets to include a header at a third format defined by a predetermined modulation at a third data rate and variable data in one of the first and second formats; and

demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

59. (Original) A method according to claim 58 wherein the predetermined modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

60. (Original) A method according to claim 55 wherein the predetermined orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

61. (Original) A method according to claim 55 wherein the predetermined orthogonal code is a bi-orthogonal code.

62. (New) A spread spectrum radio transceiver comprising:

a baseband processor and a radio circuit coupled thereto, said baseband processor comprising a demodulator for spread spectrum phase shift keying (PSK) demodulating information received from said radio circuit, at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to said radio circuit, said demodulator comprising at least one modified Walsh code function correlator for decoding information according to a modified Walsh code having a reduced DC component relative to an unmodified Walsh code for reducing an average DC signal component of the information decoded by the modified Walsh code relative to that information being decoded by the Walsh code in its unmodified state, and a modulator for spread spectrum PSK modulating information for transmission via the radio circuit, said modulator comprising at least one modified Walsh code function encoder for encoding information according to the modified Walsh code.

63. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data

rate; and wherein said demodulator is configured to operate in one of the first and second formats.

64. (New) A spread spectrum radio transceiver according to claim 63 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

65. (New) A spread spectrum radio transceiver according to claim 64 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

66. (New) A spread spectrum radio transceiver according to claim 64 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

67. (New) A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of

said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

68. (New) A spread spectrum radio transceiver according to claim 66 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

69. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one modified Walsh code function encoder.

70. (New) A spread spectrum radio transceiver according to claim 62 wherein the modified Walsh code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

71. (New) A spread spectrum radio transceiver according to claim 62 wherein said at least one modified Walsh code function correlator comprises:

a modified Walsh function generator; and

a plurality of parallel coupled correlators coupled to said modified Walsh function generator.

72. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is

configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

73. (New) A spread spectrum radio transceiver according to claim 62 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

74. (New) A spread spectrum radio transceiver according to claim 62 wherein said demodulator is configured to generate a clear channel assessment signal.

75. (New) A spread spectrum radio transceiver according to claim 62 wherein said radio circuit comprises:

a quadrature intermediate frequency modulator/demodulator coupled to said baseband processor; and

an up/down frequency converter coupled to said quadrature intermediate frequency modulator/demodulator.

76. (New) A spread spectrum radio transceiver according to claim 75 wherein said radio circuit further comprises:

a low noise amplifier having an output coupled to an input of said up/down converter; and

a radio frequency power amplifier having an input coupled to an output of said up/down converter.

77. (New) A spread spectrum radio transceiver according to claim 76 further comprising:

an antenna; and

an antenna switch for switching said antenna between the output of said radio frequency power amplifier and the input of said low noise amplifier.

78. (New) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a demodulator for spread spectrum phase shift keying (PSK) demodulating;

at least one analog-to-digital (A/D) converter having an output coupled to said demodulator and an input AC-coupled to receive information;

said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information decoded by the orthogonal code relative to that information being decoded by the orthogonal code in its unmodified state to thereby promote AC-coupling to said at least one A/D converter; and

a modulator for spread spectrum PSK modulating information for transmission, said modulator comprising at least one orthogonal code function encoder for encoding information according to the orthogonal code.

79. (New) A baseband processor according to claim 78 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate; and wherein

said demodulator is configured to operate in one of the first and second formats.

80. (New) A baseband processor according to claim 79 wherein said modulator is configured to modulate data packets to include a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and wherein said demodulator comprises is configured to demodulate data packets by demodulating the header in the third format and for switching to the respective one of the first and second formats of the variable data after the header.

81. (New) A baseband processor according to claim 80 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

82. (New) A baseband processor according to claim 80 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

83. (New) A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

84. (New) A baseband processor according to claim 82 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operating said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

85. (New) A baseband processor according to claim 78 wherein said modulator is further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder.

86. (New) A baseband processor according to claim 78 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

87. (New) A baseband processor according to claim 78 wherein the orthogonal code is a bi-orthogonal code.

88. (New) A baseband processor according to claim 78 wherein said at least one orthogonal code function correlator comprises:

a predetermined orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

89. (New) A baseband processor according to claim 78 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is configured to

generate a preamble; and wherein said demodulator comprises preamble demodulator means for demodulating the preamble for achieving initial PN sequence synchronization.

90. (New) A baseband processor according to claim 78 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

91. (New) A baseband processor for a spread spectrum radio transceiver, said baseband processor comprising:

a modulator for spread spectrum phase shift keying (PSK) modulating information for transmission, said modulator comprising

at least one encoder for encoding information for transmission,

wherein said modulator is configured to operate in one of a first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate, and

wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and

a demodulator for spread spectrum PSK demodulating received information, said demodulator comprising at least one correlator for decoding received information, wherein said demodulator is configured to operate in one of the first and second formats, wherein said demodulator is configured to demodulate data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data

after the header, a first carrier tracking loop for the third format, and a second carrier tracking loop for the first and second formats.

92. (New) A baseband processor according to claim 91 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

93. (New) A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller for selectively operating said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

94. (New) A baseband processor according to claim 91 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

95. (New) A baseband processor according to claim 91 wherein said modulator is configured to spread each data bit using a pseudorandom (PN) sequence at a chip rate and is further configured to generate a preamble; and wherein said demodulator is configured to demodulate the preamble for achieving initial PN sequence synchronization.

96. (New) A baseband processor according to claim 91 wherein said modulator comprises a scrambler; and wherein said demodulator comprises a descrambler.

97. (New) A modulator for a spread spectrum radio transceiver, said modulator configured to modulate information for transmission by spread spectrum phase shift keying (PSK), said modulator comprising at least one orthogonal code function encoder for encoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the orthogonal code relative to that information being encoded by the orthogonal code in its unmodified state.

98. (New) A modulator according to claim 97 wherein said modulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

99. (New) A modulator according to claim 98 wherein said modulator is configured to modulate data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats.

100. (New) A modulator according to claim 99 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

101. (New) A modulator according to claim 97 wherein said modulator is configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits) to said at least one orthogonal code function encoder, and wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

102. (New) A modulator according to claim 97 wherein said at least one orthogonal code function correlator comprises:

an orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

103. (New) A modulator according to claim 97 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

104. (New) A modulator according to claim 97 wherein the orthogonal code is a bi-orthogonal code.

105. (New) A demodulator for a spread spectrum radio transceiver, said demodulator configured to demodulate information by spread spectrum phase shift keying (PSK) demodulating information received from a radio circuit, said demodulator comprising at least one orthogonal code function correlator for decoding information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the

information decoded by the orthogonal code relative to that information being decoded by the orthogonal code in its unmodified state.

106. (New) A demodulator according to claim 105 wherein said demodulator is configured to operate in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

107. (New) A demodulator according to claim 106 wherein said demodulator is configured to demodulate data packets including a header in a third format defined by a modulation at a third data rate and variable data in one of the first and second formats, and for switching to the respective one of the first and second formats of the variable data after the header.

108. (New) A demodulator according to claim 107 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

109. (New) A demodulator according to claim 107 wherein said demodulator further comprises:

a first carrier tracking loop for the third format; and

a second carrier tracking loop for the first and second formats.

110. (New) A demodulator according to claim 109 wherein said second carrier tracking loop comprises:

a carrier numerically controlled oscillator (NCO); and

a controller to selectively operate said carrier NCO based upon a carrier phase of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

111. (New) A demodulator according to claim 109 wherein said second carrier tracking loop comprises:

a carrier loop filter; and

a controller to selectively operate said carrier loop filter based upon a frequency of said first carrier tracking loop to thereby facilitate switching to the format of the variable data.

112. (New) A demodulator according to claim 105 further configured to partition data into four bit nibbles of sign (one bit) and magnitude (three bits).

113. (New) A demodulator according to claim 105 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

114. (New) A demodulator according to claim 105 wherein the orthogonal code is a bi-orthogonal code.

115. (New) A demodulator according to claim 105 wherein said at least one orthogonal code function correlator comprises:

an orthogonal code function generator; and

a plurality of parallel coupled correlators coupled to said orthogonal code function generator.

116. (New) A method for spread spectrum radio communication, the method comprising:

spread spectrum phase shift keying (PSK) modulating information for transmission while encoding the information according to an orthogonal code, wherein the orthogonal code is modified to have a reduced DC component for reducing an average DC signal component of the information encoded by the orthogonal code relative to that information being encoded by the orthogonal code in its unmodified state; and

spread spectrum PSK demodulating received information by decoding the received information according to the orthogonal code.

117. (New) A method according to claim 116 further comprising AC-coupling received information for spread spectrum PSK demodulating so that the reduced average DC signal component in combination with the AC-coupling enhances overall performance.

118. (New) A method according to claim 116 further comprising modulating and demodulating in one of first format defined by bi-phase PSK (BPSK) modulation at a first data rate and a second format defined by quadrature PSK (QPSK) modulation at a second data rate.

119. (New) A method according to claim 118 further comprising:

modulating data packets to include a header at a third format defined by a modulation at a third data rate and variable data in one of the first and second formats; and

demodulating data packets by demodulating the header at the third format and for switching to the respective one of the first and second formats of the variable data after the header.

120. (New) A method according to claim 119 wherein the modulation of the third format is differential BPSK (DBPSK), and wherein the third data rate is lower than the first and second data rates.

121. (New) A method according to claim 116 wherein the orthogonal code is a Walsh code modified by a modulo two addition of a fixed hexadecimal code thereto.

122. (New) A method according to claim 116 wherein the orthogonal code is a bi-orthogonal code.

123. (New) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence generated at a predetermined chip rate;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences generated at the same chip rate as said spreading sequence and chosen from a set that is substantially orthogonal with low DC components; and

applying the spread-spectrum encoded symbols of said header field and selected chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

124. (New) The method of claim 123 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit second data symbol and differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.

125. (New) A method of generating an rf signal for transmitting binary information in a packet format including a header field followed by a data field, comprising the steps of:

spread spectrum encoding a sequence of first data symbols from said binary information within said header field by combining said first data symbols with a spreading sequence;

encoding a sequence of N-bit second data symbols, where N is greater than 1, from said binary information within said data field by generating for each of said N-bit second data symbols one of a set of 2^N chip sequences chosen from a set that is substantially orthogonal with low DC components, each of said chip sequences being differentially phase encoded;

applying a reference phase based on encoding of the last of said first data symbols to the differential encoding of the first selected chip sequence; and

inputting said encoded symbols of said header field and said differentially encoded chip sequences of said data field to the I and Q inputs of a phase shift modulator to produce said rf signal.

126. (New) The method of claim 125 wherein each said chip sequence is generated by selecting an initial chip sequence in accordance with a first data segment of an N-bit second data symbol and

differentially phase encoding said initial chip sequence in accordance with a second data segment of the same N-bit second data symbol.

127. (New) A method of generating an rf signal in a transmitter having a phase shift modulator with I and Q inputs comprising the steps of:

supplying a stream of binary information containing header data and payload data, said header data specifying at least a first payload data rate or a second payload data rate;

encoding said payload data when said header data specifies said first payload data rate by grouping said payload data into N-bit symbols, where N is greater than 1, and applying each N-bit symbol to select one of 2^N possible chip sequences and chosen from a set that is substantially orthogonal with low DC components;

encoding said payload data when said header data specifies said second payload data rate by grouping said payload data into 2N-bit symbols and applying each 2N-bit symbol to select one of 2^{2N} possible chip sequences; and

applying each selected chip sequence to the I and Q inputs of said phase shift modulator.

128. (New) The method of claim 127 wherein the chip sequences selectable by said 2N-bit symbols include the chip sequences selectable by said N-bit symbols plus 2^{2N}-2^N additional chip sequences.

129. (New) The method of claim 127 wherein the chip sequences selected by said N-bit symbols and said 2N-bit symbols are generated by selecting an initial chip sequence in accordance with a

first data segment of an N-bit or 2N-bit symbol and differentially phase encoding the selected initial chip sequence in accordance with a second data segment of the same N-bit or 2N-bit symbol.

130. (New) The method of claim 127 wherein each of the 2^{2N} chip sequences selectable by said 2N-bit symbols comprises an I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively.

131. (New) The method of claim 129 wherein N=4 and wherein each chip sequence selected by a 2N-bit symbol comprises an initial I/Q chip sequence having an I segment and a Q segment adapted to be synchronously applied to said I and Q inputs, respectively, said initial I/Q chip sequence being selected by 6 bits of a 2N-bit symbol and being differentially phase encoded in accordance with the other 2 bits of the same 2N-bit symbol.

132. (New) A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:

grouping said binary data into N-bit symbols;

applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences, wherein each chip sequence is M chips in length and is a composite of an M-bit basic sequence and an M-bit modification sequence and chosen from a set that is substantially orthogonal with low DC components;

rotating the phase of the selected chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said chip sequence; and

transmitting each phase-rotated, selected chip sequence at said predetermined chip rate.

133. (New) A method of encoding binary data for transmission in packet format along with information encoded at a predetermined spread spectrum chip rate, said method comprising the steps of:

grouping said binary data into N-bit symbols;

applying a K-bit segment of each N-bit symbol to a chip sequence generator to select one of 2^K chip sequences chosen from a set that is substantially orthogonal with low DC components, wherein each chip sequence is M chips in length;

combining the selected basic chip sequence with a fixed, M-chip modification sequence to produce a selected M-chip composite chip sequence;

rotating the phase of the selected M-chip composite chip sequence in accordance with an N-K bit segment of the same N-bit symbol that selected said basic chip sequence; and

transmitting each phase rotated, selected composite chip sequence at said predetermined chip rate.

Remarks

Claims 1-133 remain pending in this application and have been indicated as allowable. As noted above, this Supplemental Amendment does not make any changes to the claims but rather updates them to show amendments already made to the claims with respect to the issued patent claims as required of a reissue application under 37 C.F.R. § 1.121. Because the Amendment does not raise any new issues, entry is respectfully requested.

Applicant appreciates the Patent Office's indication that all pending claims 1-133 are allowable. However, in recognition of the minor formalities brought to Applicant's attention by Special Programs Examiner Zele, Applicant has amended the claims and respectfully submits that all formal matters have thereby been satisfied.

Should the Patent Office determine that anything further would be desirable in order to place this application in even better condition for allowance, the Office Personnel are invited to contact Applicant's undersigned representative at the telephone number listed below.

Applicants believe that no charges are due in connection with this amendment. However, in the event Patent Office charges are due, please charge the undersigned's Deposit Account No. 50-0206.

Respectfully submitted,

Dated: March 31, 2006

By: _____
Phillip D. Mancini
Registration No. 46,743

HUNTON & WILLIAMS
Intellectual Property Department
1900 K Street, N.W., Suite 1200
Washington, D.C. 20006-1109
(202) 955-1500 (Telephone)
(202) 778-2201 (Facsimile)

PTO/SB/51 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

REISSUE APPLICATION DECLARATION BY THE INVENTOR	Docket Number (Optional) 56162.000489

I hereby declare that:
Each inventor's residence, mailing address and citizenship are stated below next to their name.
I believe the inventors named below to be the original and first inventor(s) of the subject matter which is described and claimed in patent number 5,982,807, granted November 9, 1999 and for which a reissue patent is sought on the invention entitled High Data Rate Spread Spectrum Transceiver and Associated Methods,

the specification of which

☐ is attached hereto.

☒ was filed on 11/09/2001 as reissue application number 10/005,483

and was amended on 11/09/01; 08/28/02; 10/23/02; 12/02/02; 06/19/03; 03/05/04; 11/09/04; and 09/29/05.
(If applicable)

I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.
I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

☐ I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b). Attached is form PTO/SB/02B (or equivalent) listing the foreign applications.

I verily believe the original patent to be wholly or partly inoperative or invalid, for the reasons described below. (Check all boxes that apply.)

☐ by reason of a defective specification or drawing.

☑ by reason of the patentee claiming more or less than he had the right to claim in the patent.

☐ by reason of other errors.

At least one error upon which reissue is based is described below. If the reissue is a broadening reissue, such must be stated with an explanation as to the nature of the broadening:

This reissue application is based on an error in that the applicant and applicant's attorney failed to appreciate the full scope of the invention and thus claimed less subject matter than could have been claimed. The issued claims contain limitations that are not essential for practicing the broad teachings of the invention disclosed in the application. Thus, this reissue application is intended as a broadening reissue.

In one example of this error, in issued patent claim 2, Applicant employed means plus function language. The new claims presented in this reissue application avoid the use of means plus function language and thus broaden the scope of the invention.

PTO/SB/51 (04-05)
Approved for use through 04/30/2007. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

(REISSUE APPLICATION DECLARATION BY THE INVENTOR, page 2)

Docket Number (Optional): 56162.000489

All errors corrected in this reissue application arose without any deceptive intention on the part of the applicant.

Note: To appoint a power of attorney, use form PTO/SB/81.

Correspondence Address: Direct all communications about the application to:

☑ The address associated with Customer Number: 21967

OR

☐ Firm or Individual Name					
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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine and imprisonment, or both, under 18 U.S.C. 1001, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this declaration is directed.

Full name of sole or first inventor (given name, family name): James Leroy Snell

Inventor's signature | Date

Residence: 2695 Lemon Street, NE, Palm Bay, Florida 32905 | Citizenship: U.S.

Mailing Address: Same as above

Full name of second joint inventor (given name, family name): Carl F. Andren

Inventor's signature: Carl F. Andren | Date: 4/14/2006

Residence: 906 S. Ramona Avenue, Indialantic, Florida 32903 | Citizenship: U.S.

Mailing Address: Same as above

Full name of third joint inventor (given name, family name): Leonard Victor Lucas

Inventor's signature | Date

Residence: 11529 Greenwood Ave., N, Apt. 6, Seattle, WA 98133 | Citizenship: U.S.

Mailing Address: Same as above

☐ Additional joint inventors or legal representative(s) are named on separately numbered sheets forms PTO/SB/02A or 02LR attached hereto.

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2006 WEB TAX STATEMENT

Printed:04/13/2006

LUCAS VICTOR L
7106 SE SEDGWICK
PORT ORCHARD, WA 98366

For Informational Purposes Only

Account Number	Process Number	Taxpayer Name:
092302-2-001-2003	1081405	LUCAS VICTOR L

Tax Property Description

09232E
THE NE1/4 NE1/4 NW1/4 CNVYD BY AUD NO. 1103022 EXC FDT, BAT NE COR OF SD NE1/4 NE1/4 NW1/4 TH S0°55'48W ALG E LN THOF 30.00FT TO TPOB OF TH EXC TH N87°56'03W 150.04FT THE S0°55'48W 157.21FT TH S21° 08'20E 87.27FT TH S87°56'03E 108.00FT TH N0°55'48E 260.05FT TO TPOB ALSO EXC FDT, BAT NE COR OF SD NE1/4 NE1/4 NW1/4 TH S0°55'48W 290.55FT TO TPOB TH CONT S0°55'48W 80.00FT TH N87°56'03W 54.66FT TH IN A NWLY DIR 86.42FT M/L TAP TH IS N87°56'03W 87.36FT FD TPOB TH S87°56'03E 87.36FT TO TPOB & EXC RD

GENERAL TAX DISTRIBUTION

2005		2006	
STATE GENERAL	$568.37	STATE GENERAL	$580.77
REGIONAL LIBRARY	$80.55	REGIONAL LIBRARY	$80.80
LOCAL SCHOOL	$538.52	LOCAL SCHOOL	$558.74
COUNTY	$251.17	COUNTY	$252.73
COUNTY ROAD	$329.79	COUNTY ROAD	$329.51
FIRE	$328.42	FIRE	$338.98
PUD	$17.70	PUD	$17.81
2005 Total:	$2,114.52	2006 Total:	$2,159.34

VALUE INFORMATION FOR TAX

	2005	2006
Land:	$71,270	$89,090
Improvements:	$120,680	$134,360
TOTAL VALUE:	$191,950	$223,450
Frozen Base:	$0	$0
Exemptions (if any):		
Total Qualifying Exemptions:	$0	$0

TOTAL TAXABLE VALUE:(Land + Improvements minus Qualifying Exemptions)

2005	2006
$191,950	$223,450

Levy Code 8320 — General Levy Rate per $1000 9.6637

Voted Rate – 25.9 % Voter Approved

Current Taxes

ASSESSMENT	2005	2006
Noxious Weed	$1.60	$1.60
Stormwater Management	$47.50	$50.00
Asmt Total	$49.10	$51.60

2006 General Property Tax + Assessments = $2,210.94

Delinquent Section		
Year	Taxes Int/Pen to 4/2006	Total
Total Delinquent Amt Due:		$.00
Total Collection Cost:		$.00

TOTAL AMOUNT DUE: $2,210.94

First half taxes paid after April 30th will incur interest plus penalty computed on the FULL year amount (RCW 84.56.020).

Account Number: 092302-2-001-2003 (1081405)

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2

LUCAS VICTOR L
7106 SE SEDGWICK
PORT ORCHARD, WA 98366

SECOND HALF - Pay or Postmark by October 31

	TAX YEAR	Prev Tax Owing	Interest/ Penalty	TOTAL Full	TOTAL Half
Current:	2006				$1,105.47
					$.00
Delinquent					
		Amount Due:			$1,105.47

Make Remittance Payable To
Kitsap County Treasurer - PO Box 34303 - Seattle, WA 98124

Tax Statement

Account Number: 092302-2-001-2003 (1081405)

Parcel Location: 7106 SE SEDGWICK RD

Payments of prior year taxes must include all interest and penalty due. Delinquent payments received without interest and penalty will be returned. See Treasurer Information link.

1

LUCAS VICTOR L
7106 SE SEDGWICK
PORT ORCHARD, WA 98366

FIRST HALF - Pay or Postmark by April 30

	TAX YEAR	Prev Tax Owing	Interest/ Penalty	TOTAL Full	TOTAL Half
Current:	2006			$2,210.94	$1,105.47
Collection				$.00	
		Amount Due:			$1,105.47

Make Remittance Payable To
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